Quantum Multiplexer: A novel device architecture for low-temperature measurements

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Abstract

We present a quantum device architecture which significantly increases the number of electrical contacts locally available on a single chip, without modification of existing experimental setups. We use the quantum multiplexer to measure 256 quantum wires formed by split-gate devices with common source-drain contacts, on a single chip using only 19 electrical contacts. This is currently the largest number of split-gate devices measured on a single chip on a single cool down. After illumination, the mean and standard deviation of the channel pinch-off voltage increased by a factor of 3.5 and 1.5, respectively. The multiplexer is a scalable architecture and is fabricated using standard clean-room techniques. It can be extended to the measurement of more complex quantum devices including zero-dimensional quantum dots, parallel charge pumps and studies on quantum devices for application in integrated circuits.

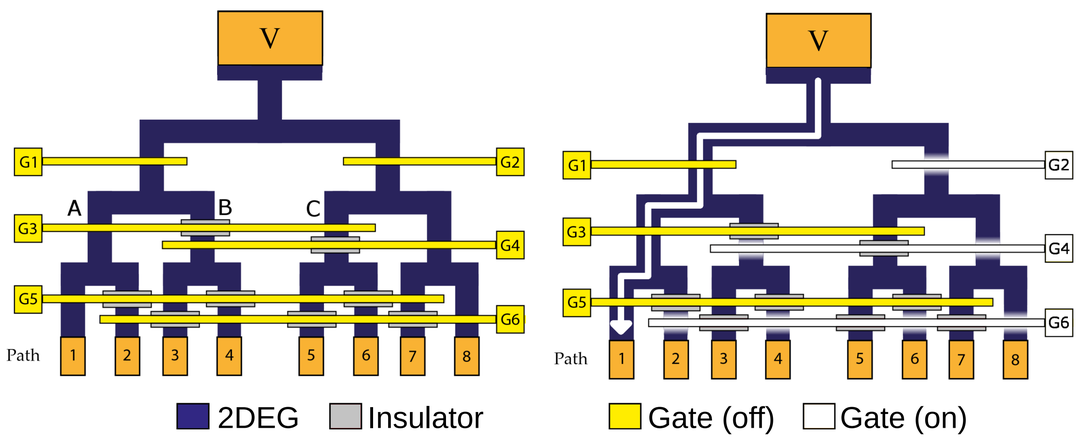
1. Current Research Limitations

- The number of quantum devices and device complexity on a single chip is limited.
- This limitation set by small number of electrical contacts on a cryogenic measurement system.
- In order to measure more devices, an increase in the number of electrical wires available in the measurement setup would be a possible solution. However, this approach results in a greater heat load in the system.
- Low-temperature research
  - Slow
  - Expensive
  - Time-consuming

Therefore, a local increase in the number of electrical contacts available on a single chip without modification of existing fabrication or cryogenic setups is highly desirable.

- This allows a detailed statistical study of yield, manufacturability and reproducibility of device characteristics to be undertaken, and proves that such devices can be integrated into a scalable architecture.

2. Quantum Multiplexer



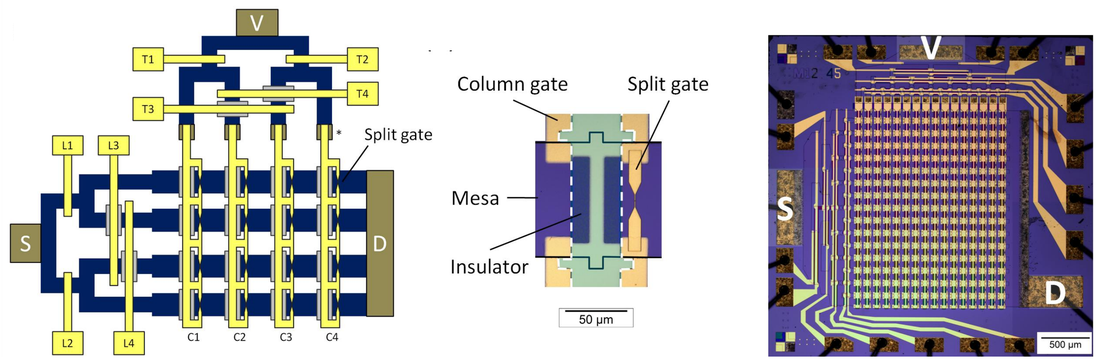
- Spin-coated insulator (Polyimide) at B alters the pinch-off voltage such that a negative voltage applied to G3 is sufficient to deplete the 2DEG at A and C but not B.
- If addressing gates G2, G4 and G6 are ‘on’, voltage at V is directed to path 1.
- A voltage offset must be maintained between each addressing gate and the potential applied at V, where the offset voltage is the potential required to address a particular path when the potential at V is zero.
- The voltage path is altered depending on which gates are ‘on’ and ‘off’.
- Number of multiplexer output paths is given by

$$N_{mux} = 2^{(n-1)/2}$$

where n = number of physical addressing and input contacts required.

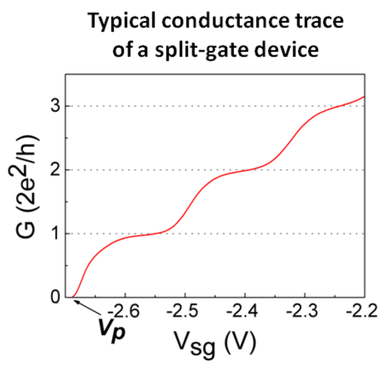
3. Application

- Split gates are the simplest mesoscopic devices to exhibit quantum phenomena and are the building block for more complex devices, such as quantum dots.
- The measurement of 256 (16 x 16) split-gate devices on a GaAs/AlGaAs High Electron Mobility Transistor (HEMT) heterostructure is presented.
- Left multiplexer addresses channel (mesa) row and directs an excitation voltage.
- Top multiplexer addresses and directs a gate voltage (V) column.
- Individual measurement of split-gate devices is possible by appropriately addressing both multiplexers to select a particular row and column.



4. Results

- Largest number of split-gate devices measured on a single chip, on a single cool down.
- 241 split-gate devices show channel pinch off , when conductance (G) as a function of split-gate voltage (V_{sg}) is zero, indicated by V_p.
- The sample is illuminated to saturation.
- After illumination, an increase in mean (μ) and standard deviation (σ) of the channel pinch-off by a factor of 3.5 and 1.5, respectively is observed.
- The increase in mean is due to an increase in 2DEG carrier concentration and mobility.
- Although there is an increase in the absolute value of σ, there is a reduction in the percentage variation from the mean. This is maybe related to the reduced impurity effects leading to less disorder in the 1D channel after illumination.



Future Work

- Further statistical analysis on split-gate physics.
- Statistical device analysis on 0D quantum dots.
- Parallel charge pumps.
- Study of quantum integrated circuits.

[1] – H. Al-Taie *et al.*, Appl. Phys. Lett. **102**, 243102 (2013).
[2] – Q. -Z.Yang *et al.*, Appl. Phys. Lett. **94**, 033502 (2009).

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