Towards nano-structure circuits using split gates

L. W. Smith[1], H. Al-Taie[1,2], B. Xu[1], J. P. Griffiths[1], H. E. Beere[1], G. A. C. Jones[1], D. A. Ritchie[1], C. G. Smith[1], and M. J. Kelly[1,2]

[1] *Cavendish Laboratory, J. J. Thomson Avenue, Cambridge, CB3 0HE, United Kingdom*
[2] *Centre for Advanced Photonics and Electronics, Department of Engineering, University of Cambridge, 9 J. J. Thomson Avenue, Cambridge, CB3 0FA, United Kingdom*

It is hard to underestimate the importance of the simple split-gate in the world of mesoscopic devices. It was using split gates that the conductance through a one-dimensional (1D) constriction was first shown to be quantised in units of $2e^2/h$. Since then, split gates fabricated on GaAs heterostructures have been ubiquitous in 1D physics, facilitating a vast amount of research on quantum phenomena.

It has recently been demonstrated that split gates can be used as an electrical means of generating a spin-polarized current, which has potential application in the emerging field of 'spintronics', where information is transferred in a circuit using the spin state of electrons [1, 2]. However, in order for split gates to be used in larger, more complex circuits, the scalability of this technology must be considered; it should be shown that electrical characteristics are highly consistent from device to device.

We have fabricated 256 lithographically-defined split gates on a single chip, by developing a novel device layout which enables selective contact to each split gate individually. Our split-gate yield was better than 94%, and we measured more than 600 nominally-identical devices fabricated on two different GaAs/AlGaAs wafers. We compare the conductance through the split gates before and after thermal cycling, as well as before and after illumination, and show how the quality of the conductance quantisation is affected by carrier density and mobility, impurity scattering, background-potential variations, and split-gate roughness. This is the first real test of the reproducibility of the electrical characteristics of a large number of split gates, inspired by initial work by Yang *et al.* [3], which was limited in the number of split gates that could be measured on a single cool down. We will also present statistical variations in the occurrence of the '0.25 feature', which appears at $0.25 \times (2e^2/h)$ when a large dc bias is applied across the split gate [4]. The 0.25 feature has the characteristics of being spin polarised, and as such has potential as an electrically-controlled spin injector in spintronic applications [2].

Our array of split-gate devices is a powerful tool. It tests the quality of the underlying GaAs wafer, since it is possible to determine the probability of encountering an impurity in the 1D channel, and hence an estimate of the impurity density. In addition, a systematic study of statical variations in the occurrence of conductance anomalies − such as the 0.7 structure and zero bias anomaly − can be performed for the first time. This will be instructive, since a definitive explanation for these conductance anomalies remains to be given.

[1] P. Debray, S. M. S Rahman, J. Wan, R. S. Newrock, M. Cahay, A. T. Ngo, S. E. Ulloa, S. T. Herbert, M. Muhammad, and M. Johnson, Nature Nanotech. **4**, 759 (2009).

[2] T.-M. Chen, M. Pepper, I. Farrer, G. A. C. Jones, and D. A. Ritchie, Phys. Rev. Lett. **109**, 177202 (2012).

[3] Q.-Z. Yang, M. J. Kelly, I. Farrer, H. E. Beere, and G. A. C. Jones, Appl. Phys. Lett. **94**, 033502 (2009).

[4] T.-M. Chen, A. C. Graham, M. Pepper, I. Farrer, and D. A. Ritchie, , Appl. Phys. Lett. **93**, 032102 (2008).